

# ANAND MANDAPATI

3623 18<sup>th</sup> St., #2  
San Francisco, CA 94110

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## SUMMARY

- Proven leader of large-scale projects from specification to final product.
- Very proficient in all stages of VLSI hardware design including specification, architecture, design, implementation, verification, and productization.
- Excellent communicator, problem solver, and technical lead.
- Experienced with writing system, user application, and EDA software.

## EXPERIENCE

10/06 - present

**Director of Engineering, Advanced Micro Devices, Inc., Santa Clara, CA, Graphics Product Group, Visual and Media Business Unit.**

[ati.com](http://ati.com)

AMD acquired ATI in October 2006.

- Playing key role in the management team responsible for integrating ATI and AMD after acquisition, ranging from being member of IT Steering Committee to decide on IT strategy for combined company and setting up processes for export controls and licenses for business unit to helping select process for company-wide Fusion projects.

9/03 - 10/06

**Director of Engineering, ATI Technologies, Inc., Santa Clara, CA, Discrete Graphics Hardware, PC Business Unit.**

[ati.com](http://ati.com)

ATI designs and manufactures video graphics and multimedia hardware.

- Managing all technical and operational aspects of multiple high-performance desktop & mobile discrete graphics processor designs. To date, have managed designs of 21 GPUs (e.g., Radeon X1300, X1950, etc.) including as many as 10 concurrently with as many as 700M+ transistors. Revenues for most of the above GPUs are in the multiple \$100M range each with annual totals in the \$1.3-1.9B range.
- Coordinating architecture, technology, and operational teams to specify architectures, process technologies, and performance, power & cost targets for designs.
- Managing multiple logic & physical design, integration, DFT, and verification teams, ranging from 15-75 people per project, to implement above GPU designs.
- Coordinating internal & external IP vendors, marketing teams, package, board, & software design teams, bringup & qualification teams, and external vendors including foundries to bring above GPU designs to market.
- Serving as technical contact within company for 110nm, 80nm, 65nm, and 55nm process generations as well as assisting on 130nm, 90nm, and 45nm generations.
- Leading discussions with marketing and executive teams to generate roadmap for future generations of products.

3/03 – 8/03

**CAD & Physical Design Engineer, Azul Systems, Inc., Mountain View, CA.**

[azulsystems.com](http://azulsystems.com)

Azul Systems is an enterprise IT infrastructure startup.

- Led CAD and physical design activities for a large COT ASIC.

7/02 – 3/03

**Consultant, Rapid Silicon Co., San Francisco, CA.**

[rapidsi.com](http://rapidsi.com)

Rapid Silicon provides consulting services for VLSI design.

- Provided VLSI design consulting services in support of multiple ASICs.

4/00 – 4/01

**CAD & Physical Design Manager, ATI Technologies, Inc., Santa Clara, CA.**

[ati.com](http://ati.com)

ATI Technologies acquired ArtX in April 2000 to gain access to our engineering talent and product portfolio.

- Played key role in the management team responsible for integrating ArtX and ATI Technologies design teams and methodologies after acquisition.
- Expanded role as CAD & physical design manager of entire Santa Clara site.

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8/98 – 4/00

## **CAD & Physical Design Manager, ArtX, Inc., Palo Alto, CA.**

ArtX was a startup company that designed video graphics hardware for highly integrated low-cost PCs and for the Nintendo GameCube video game console.

[ati.com/  
companyinfo/ir/  
2000/2000.html](http://ati.com/companyinfo/ir/2000/2000.html)

- Managed team responsible for all physical implementation activities of three multi-million gate COT ASICs that combined graphics, CPU controller, and memory controller, for PCs and the Nintendo GameCube.
- Managed relationships with various EDA tool vendors, library vendors, contractors, foundries, and high-profile customers such as Nintendo.
- Performed various logic & physical design & verification tasks using third-party vendor and internally developed tools for multiple tapeouts.
- Developed methodologies and CAD tools to aid in synthesis, DFT, integration, floorplanning, place & route, timing analysis, and physical verification.

1/95 – 7/98

## **Staff Engineer, IBM Corp., Somerset Design Center, Austin, TX, PowerPC Processor Development, Microelectronics Division.**

The Somerset Design Center was a joint effort staffed by IBM and Motorola engineers developing microprocessors for the Apple Macintosh product line.

[ibm.com](http://ibm.com)

- PowerPC G4 - microarchitected, designed, verified, timed and floorplanned load/store/memory subsystem for G4 series of microprocessors.
- PowerPC 620 - designed and verified data cache & memory management units and array BIST of various arrays; performed hardware bringup & debug; developed PowerPC hardware simulation models for external customers.
- Developed various tools, scripts, and graphical user interfaces.

9/94 - 1/95

## **Engineer, VLSI Technology, Inc., Tempe, AZ, ASIC Core Technology.**

- Developed X Window/Motif user interfaces for ASIC design toolkit.

[vlsi.com](http://vlsi.com)

3/93 - 4/94

## **Contract Engineer/Programmer, Dell Computer Corp., Austin, TX, Advanced Systems Development.**

- Wrote portions of PC BIOS; designed PCBs; wrote system utilities in C/C++

[dell.com](http://dell.com)

1/92 - 12/92

## **Contract Engineer, Advanced Micro Devices Corp., Austin, TX, PC Division.**

- Am486 - generated microcode blocks; wrote various CAD tools in C.

[amd.com](http://amd.com)

## **SKILLS**

**EDA Tools:** Proficient in most major design and verification tools from Cadence, Synopsys, Mentor Graphics, Avant!, Get2Chip, Silicon Canvas, Simplex, Verplex, Silicon Perspective, IBM, COMPASS, ViewLogic, Zycad, and UC Berkeley.

**Languages:** Verilog, C, C++, PowerPC, Intel x86, and Motorola 68xxx assembly languages, Perl, Tcl/Tk, HTML, JavaScript, AppleScript.

**Other:** UNIX system, network & Web server administration.

## **EDUCATION**

8/95-5/97

National Technological University, MS Computer Engineering (incomplete).

8/94

University of Texas at Austin, BS Electrical Engineering (Computer Block).